In the Claims:

1-20. (canceled)

21. (new) Circuitry comprising:

A. plural data output paths, each path including a tri-state output buffer having a data input, a data output and a control input;

B. a control signal input path including an input buffer having a signal input and a signal output; and

C. a scan path between a test data input lead and a test data output lead, including:

i. a first scan cell having a functional data input connected to the signal output of the input buffer, a functional data output connected to the control inputs of all the output buffers, a test data input coupled to the test data input lead, and a test data output separate from the functional data output;

ii. second scan cells, each second scan cell having a functional data input, a test data input, and a combined data output of functional data and test data, the second scan cells being connected in a series with the test data input of the initial second scan cell in the series being connected to the test data output of the first scan cell, and the combined data output of each second scan cell being connected to the test data input of the next, successive second scan cell, the combined data output of each second scan cell also being directly connected to the data input of one tri-state output buffer; and

iii. multiplexer circuitry having one input connected to the combined data output of the last second scan cell in the series, another input connected to the test data output of the first scan cell, and an output coupled to the test data output lead.

22. (new) The circuitry of claim 21 in which the first scan cell includes an input multiplexer having an input connected to the functional data input, another input connected to the test data output, and an output, a first memory having an input connected to the output of the input multiplexer and an output connected to the test data output, a second memory having an input connected to the output of the first memory and an output, and an output multiplexer having an input connected to the functional data input, another input connected to the output of the second memory, and an output connected to the functional data output.

23. (new) The circuitry of claim 21 in which each second scan cell includes an input multiplexer having an input connected to the functional data input, another input connected to the test data input, and an output, and a memory having an input connected to the output of the input multiplexer and an output connected to the combined data output.

24. (new) The circuitry of claim 21 in which the circuitry is part of a master and slave integrated circuit.